B.E. / B.Tech. Electronics & Communication / Telecommunication Engineering
(Model Curriculum) Semester-III

SE103 / 003 - Digital System Design

P. Pages : 2 **GUG/S/25/13908**

Time : Three Hours * 2 3 1 8 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Assume suitable data wherever necessary.
3. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Simplify $Y = A + B(AC + (B + C')D)$ using Boolean algebra. **4**

b) Solve **4**

i) $(2777)_{10} = (?)_8 = (?)_{16}$

ii) $(100.425)_{10} = (?)_5$

c) Minimize using K-map F = **8**

$F = AB + AC' + C + AD + AB'C + ABC$

OR

2. a) Minimize using K-Map $F = \sum m(0,2,5,9,15) \cdot d(6,7,8,10,12,13)$ and implement using NOR only. **8**

b) Simplify the logic function $F(A,B,C) = \sum m(3,5,6,11,13,14,15) + d(4,9,10)$ using K-map in SOP and POS form implement using basic gate. **8**

3. a) Draw 1:8 Demux using 1:2 Demux only **4**

b) Implement the following functions using a 3-to-8 decoder **6**
$F1(A,B,C) = AB + A'B'C'; F2(A,B,C) = A'B + AB'$.

c) Design full adder with K-map for Sum and Carry. **6**

OR

4. a) Design Moore Type Serial Adder. **8**

b) Define Encoder? Implement an Octal to binary encoder. **8**

5. a) Convert D Flip Flop to T Flip Flop. **6**

b) Design a MOD-6 counter using JK Flip Flop with separate logic circuitry for each J and K input? Construct a state diagram to determine whether the counter is self stating or not. **10**

OR

6.	a)	What is race around condition in JK Flip-Flop? Explain Master-Slave JK Flip-Flop with characteristic & Excitation table.	**8**
	b)	Design a sequence generator that generates the sequence "100010011010111"	**8**
7.	a)	Explain CMOS NAND and NOR gate with 2-input.	**8**
	b)	Implement BCD to Excess-3 code convertor using bipolar transistor PROM.	**8**

OR

8.	a)	Explain the classification of memory.	**6**
	b)	Design a 2-bit comparator using PLA.	**10**
9.	a)	What is identifier? State the rule governing identifier.	**4**
	b)	Write the VHDL code of full adder in structural design style using 2-input NAND gate only as component.	**12**

OR

10.	a)	If A = "110", B = "111", C = "011000" and D = "111011", compute the following (A & not B or C ror 2 and D)	**4**
	b)	If A = "101", B = "011" and C = "010". What are the values of the following statements (i) (A & B) OR (B & C); (ii) A OR B AND C;	**4**
	c)	Discuss about signal assignments with examples in VHDL.	**8**

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